WHAT IS CLAIMED IS:

1. A semiconductor chip comprising:

a delay monitoring means for finding a critical path delay characteristic of a target circuit subjected by power supply voltage control;

a voltage setting signal generating means for generating a voltage setting signal for setting a power supply voltage to be supplied to the target circuit based on the result of monitoring of delay by the delay monitoring means; and

a voltage setting restricting means for restricting the maximum value of the power supply voltage set in the voltage setting signal to a predetermined value.

2. A semiconductor chip as set forth in claim 1, wherein said voltage setting restricting means comprises:

a first storing means for storing a maximum voltage setting signal for setting the maximum value of the power supply voltage to be restricted, and

a comparing means for comparing the maximum value of the power supply voltage set by the maximum voltage setting signal stored in the first storing means with the value of the power supply voltage set by the voltage setting signal and outputting the signal having a lower voltage setting.

3. A semiconductor chip as set forth in claim 2, wherein said first storing means is able to electrically erase and rewrite the stored signals.

4. A semiconductor chip as set forth in claim 2, wherein said first storing means includes one or more fuse circuits and stores signals according to a conductive state or a nonconductive state of the fuse in the fuse circuits.

5. A semiconductor chip as set forth in claim 3, further comprising:

a second storing means for storing a plurality of maximum voltage setting signals, and

a maximum voltage signal transferring means for reading out a maximum voltage setting signal selected in accordance with the signal indicating the operation state of the target circuit from the second storing means and transferring the same to the first storing means.

6. A semiconductor chip as set forth in claim 1, wherein said voltage setting restricting means determines the maximum value of the power supply voltage to be restricted in accordance with a signal indicating an operation state of the target circuit.

7. A semiconductor chip as set forth in claim 6, wherein said voltage setting restricting means includes:

a plurality of first storing means for

storing maximum voltage setting signals for setting the maximum value of the power supply voltage to be restricted;

a selecting means for selecting a maximum voltage setting signal corresponding to a signal indicating the operation state of the target circuit from among the maximum voltage setting signals stored in the plurality of first storing means; and

a comparing means for comparing the maximum value of the power supply voltage set by the maximum voltage setting signal selected by the selecting means with the value of the power supply voltage set by the voltage setting signal and outputting the signal having a lower voltage setting.

8. A semiconductor chip as set forth in claim 7, wherein said first storing means is able to electrically erase and rewrite the stored signals.

9. A semiconductor chip as set forth in claim 7, wherein said first storing means includes one or more fuse circuits and stores signals according to a conductive state or a nonconductive state of the fuse of the fuse circuits.